

**REMARKS**

Reconsideration and allowance of the present application are respectfully requested. Claims 1-18 remain pending in the application.

Applicant notes with appreciation the indication in numbered paragraph 9 of the Office Action that claims 11 and 18 contain allowable subject matter. Accordingly, the features addressed by claims 11 and 18 have, in a slightly broader aspect, been incorporated in independent claims 1 and 12, such that these claims are considered allowable.

In paragraph 3 of the Office Action, claims 1-10 and 12-17 were rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,334,175 (Chih). This rejection is respectfully traversed, because as apparently recognized by the Examiner, the Chih patent fails to teach or suggest, decoupling a first portion of a memory from the bus of a central processing unit (CPU) system, and appending the decoupled first portion to the memory with an address range which **maintains** the allocated memory **contiguous** within the memory. This feature encompasses the recitation in allowable claims 11 and 18.

For example, claim 11 recites appending the decoupled first portion of the memory to the memory at the last address. Such a feature reflects the ability of the claim 1 method to achieve the organization of a memory as illustrated, for example, in Figures 6A and 6B. In this example, memory blocks which have been decoupled from a CPU bus are assigned a last address of the memory as illustrated in blocks 635, 640 and 645 of Figure 6B, and as discussed with respect to Step 405 of Figure 4 in paragraph [0035] on page 14 of the specification.

Exemplary embodiments are directed to managing an allocation of a portion of a memory that can be selectively coupled to the bus of the CPU. Referring to Figure 6A, the memory blocks of a memory pool 610 are electrically detached and disconnected from a CPU bus 605. In step 620, a first process requests access to memory blocks of the memory, and in response, blocks E and F are allocated and electrically attached to bus 605. In steps 625 and 630, second and third processes request memory space and blocks C, D, A, and B, respectively, are allocated and electrically attached to the bus 605.

In step 635 of Figure 6B, the first process terminates memory and blocks E and F are electrically decoupled from the bus, deallocated and returned to the memory pool 610. The memory blocks are appended to the memory at the last free address of the memory, in a manner as discussed with respect to step 405 of Figure 4 in paragraph [0035]. This portion of the specification describes that a last address of memory is assigned to the decoupled first portion of memory. This portion of the specification describes that the last address in memory is the last free address in the pool of available memory.

As described in the last sentence on specification page 16, addresses of memory which have been deallocated are changed, so that deallocated memory blocks are maintained at contiguous address locations in memory. Thus, in step 640 of Figure 6B, when the third process terminates, memory blocks A and B are electrically decoupled from the bus, deallocated and returned to memory pool 610 at address locations which are contiguous with the address locations of memory blocks E and F. In step 645, when a fourth process requests three memory blocks,

contiguous blocks F, A and B can be allocated and electrically attached to the bus 605 as described on specification page 16.

The foregoing features are broadly encompassed by independent claims 1 and 12. For example, claim 1 is directed to a method for managing an allocation of a portion of a memory associated with a central processing unit system that can be selectively coupled to a bus of the central processing unit system. The claim 1 method includes, among other features, decoupling a selectively coupled first portion of the memory from the bus of the central processing unit system; and appending the decoupled first portion to the memory with an address range which **maintains** deallocated memory **contiguous** within the memory. Claim 1 further recites reallocating the decoupled first portion of the memory for a second range of addresses.

Such features are neither taught nor suggested by the Chih patent, as apparently recognized by the Examiner. The Chih patent abstract describes a memory allocator which employs a programmable and controllable switching circuit which switches multiple address buses and multiple data buses to different banks of memory depending upon determined system requirement data. FIG. 1a shows a memory allocator 100 having a processor 102 connected with multiple address buses and data buses 104a, 104b and 104c. Memory space is indicated as 106a, 106b and 106c. Address and data bus 104a corresponds with memory space 106a, address and data bus 104b corresponds with memory space 106b, and address and data bus 104c corresponds with memory space 106c. However, the memory allocator 104 includes a multiport switching circuit for each bank of memory in each

type of memory space 106a-106c. The multiport switching circuit is represented by the blocks 116a-116f.

In operation, address and data bus 104a is selected to correspond to memory space 106a by default, (see Col. 4, lines 12-14). However, if a portion of this memory space is needed as data memory, bus pairs 104b and 104c can be connected via switching circuit 116a. (see Col. 4, lines 14-17).

In operation, when notification is provided that a given application is to run, the processor 102 determines the memory allocation requirement data for that application. The allocation requirement data is used to determine whether the corresponding memory pool, for each given memory type, will satisfy the memory allocation requirement data as described at col. 5, lines 41-45. As described at col. 6, lines 4-9, if the current corresponding memory type with the corresponding address and data buses do not satisfy the memory allocation requirement data, the selector 122 looks at an update memory usage status table to determine whether other banks of memory are available in other memory spaces of the processor 102 as shown in block 214. If so, multiplexers 116A-116F are used to select appropriate banks of memory. However, the Chih patent does not disclose or suggest that deallocated portions of memory are **maintained at contiguous address locations** within memory.

As such, the Chih patent fails to teach or suggest Applicant's independent claim 1 combination of features, and this claim is considered allowable. Independent claim 12 recites features similar to those discussed with respect to claim 1 and it is also considered allowable.

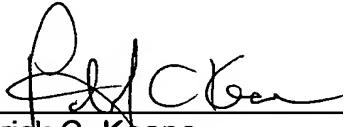
All remaining claims depend from independent claims 1 and 12, and like claims 11 and 18, are considered allowable.

All objections and rejections in the Office Action having been address, it is respectfully requested that the present application is in condition for allowance and a Notice of allowance is respectfully requested.

Respectfully submitted,

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